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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,785	DATE, ATSUSHI	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/10/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, and 7-9 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 12/10/2008, RCE, Amendment, and Extension of Time as received on 1/30/2009, and Supplemental Amendment as received on 2/10/1009.

Specification

3. The amended title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Applicant should incorporate, into the title, how exclusive access is granted.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed cross-bar switch comprising the first port and second port of claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 4, and 7-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the examiner has been unable to find support in the original disclosure for a cross-bar switch comprising a first port connected to the memory controller and a second port connected to the processor bus, the external bus interface using the processor bus and the second port of the cross-bar switch, and the built-in processor using the processor bus

and the second port of the cross-bar switch. Applicant is asked to point the examiner to specific portions of the specification and drawings which show support for such features set forth in claim 1. Otherwise, they should be canceled from claim 1.

7. Claims 4 and 7-9 are rejected under 35 U.S.C. 112, 1st paragraph, for lacking written description, because they are each dependent on a claim lacking written description.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, U.S. Patent No. 4,065,809, in view of Guttag, U.S. Patent No. 4,521,852. In addition, Yabushita et al., U.S. Patent No. 5,214,775 (herein referred to as Yabushita), is herein used as extrinsic evidence for showing that processors on separate chips may share a memory found on one of the chips.

10. Referring to claim 1, Matsumoto has taught a processor system comprising:

a) a single semiconductor substrate on which is provided a built-in processor (Fig.1, component 11), a memory controller (a system with memory inherently has a memory controller to control accesses to the memory), and a connection unit that mutually connects the memory controller and a processor bus (a processor bus is inherently connected to memory via the memory controller so that instructions/data may be obtained for processing).

b) Matsumoto has taught a second processor on the substrate (Fig.1, component 12). Matsumoto has not taught that the single semiconductor substrate includes an external bus interface to which an external processor is connected from outside of the single semiconductor substrate, the processor bus being connected with the first processor and the external bus interface. However, Guttag has taught a chip including a built-in processor and an external bus interface through which peripherals communicate with components on chip. See Fig.1 and column 3, line 41, to column 4, line 39. The examiner asserts that any parts may be integrated on a single chip or made separate, as integration and separation of parts are well known and not patentable features. See *In re Larson 144 USPQ 347 (CCPA 1965)* and *Nerwin v. Erlichman 168 USPQ 177 (1969)*. As a result, since separation of parts is a non-patentable feature, it would have been obvious to one of ordinary skill in the art to modify Matsumoto in view of Guttag such that the single semiconductor substrate includes an external bus interface to which the second processor (Matsumoto, Fig.1, component 12) is connected from outside of the single semiconductor substrate, the processor bus being connected with the first processor and the external bus interface. It should be noted that, while Guttag does not explicitly disclose that a peripheral is an external processor, it is known that an external processor can access another processor's on-chip memory. For instance, see Yabushita, Fig.1, Fig.10, the abstract, column 2, lines 65-68, and claim 11, which provides a specific teaching of a processor and shared memory on a single chip and a processor external to the chip which communicates with the shared memory via an external interface. Hence, given each of these teachings, separating processor 12 of Matsumoto out onto another chip and allowing it to access the memory 19 through an external bus interface would have been obvious.

c) Matsumoto, as modified, has not taught that the connection unit is a cross-bar switch comprising at least a first port connected to the memory controller and a second port connected to the processor bus. However, crossbar switches and their advantages are well known and accepted in the art. A crossbar switch is useful because as the traffic between any two devices increases, it does not affect traffic between other devices. In addition, it is much more scalable than a traditional bus. Consequently, to reduce traffic and increase scalability, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto such that the connection unit is a crossbar switch with ports coupled to the bus and memory controller.

d) Matsumoto, as modified, has further taught that first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, wherein the first enable signal is asserted while the second enable signal is deasserted, so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external bus interface can use the processor bus and the second port of the cross-bar switch exclusively, and wherein the second enable signal is asserted while the first enable signal is deasserted, so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external bus interface and the built-in processor can use the processor bus and the second port of the cross-bar switch exclusively. See Fig.1 and the abstract of Matsumoto, and note the WAITa and WAITb signals. Also, see column 4, lines 56-63, and column 6, lines 42-48. When one WAIT signal is asserted the other is deasserted so that there is no bus contention between two processors when a memory access is requested. Note that Matsumoto, as modified in view

of Guttag, would send the WAITb signal to the external bus interface, much like the inhibit signal of Guttag is sent to the external bus interface in Fig.1, so that the peripheral processor's request to communicate on-chip is either granted or suppressed.

11. Referring to claim 7, Matsumoto, as modified, has taught the processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the cross-bar switch. See Fig.1 of Guttag, and recall that when Matsumoto is modified to include the external bus interface, such a common bus would exist in order to share memory accesses on a single bus, as set forth in Matsumoto.

12. Claims 4 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Guttag, and further in view of the examiner's taking of Official Notice.

13. Referring to claim 4, Matsumoto, as modified, has taught the processor system according to claim 1. Matsumoto, as modified, has not taught a second built-in processor connected to the cross-bar switch on the semiconductor substrate. However, systems having multiple processors or being scaled to include multiple processors is known in the art and advantageous because more processors yield more processing power, and throughput. Consequently, in order to increase performance, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto to include a second built-in processor connected to the connection unit on the semiconductor substrate.

14. Referring to claim 8, Matsumoto, as modified, has taught the processor system according to claim 1. Matsumoto, as modified, has not taught that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

However, it is knows that a single program may be broken up into pieces to be executed by multiple processors, thereby speeding up execution of that single program. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto such that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

15. Referring to claim 9, Matsumoto, as modified, has taught the processor system according to claim 1. Matsumoto, as modified, has not taught an image data transfer bus connected with the cross-bar switch, nor has Matsumoto, as modified, taught an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate. However, image processing is well known in the art, and in order to obtain image processing functionality in the system of Matsumoto, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto to include an image data transfer bus and an image output device interface or image input device interface so that images may be transferred to and from the processor for or after processing.

Response to Arguments

16. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
March 25, 2009